REMARKS

Claim 34 is amended. Claim 26-47 remain in the application for consideration.

Applicant hereby affirms the election made to prosecute the invention of Species I, claims 26-37. At least claims 26 and 33 are generic to Species I and II. Upon allowance of said claims as argued herein, examination of claims 38-47 is warranted and requested.

The title is amended as requested.

Claim 34 is amended to overcome the Examiner's §112 rejection. Withdrawal of same is therefore warranted.

Independent claim 26 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Background of the Invention in view of IBM Corp., *Stacked Capacitor DRAM Cell With Vertical Fins (VF-STC)*, 33 IBM Technical Disclosure Bulletin, No. 2, pp. 245-247 (July 1990). Applicant disagrees and requests reconsideration.

The Examiner is reminded that under MPEP § 706.02(j) when references are combined to show obviousness, the combined references must teach or suggest all of the limitations of the claim.

Applicant's claim 26 in part recites a well formed in an insulative layer, with the well having a base received over word lines. The well peripherally defines an outline of a memory cell area. The Examiner is mistaken that the IBM reference discloses at least these attributes of independent claim 26.

Specifically, there is no well formed in the IBM CVD oxide having a base received over wordlines. The openings formed within the IBM oxide layer are contact openings, not wells, and regardless such don't have a "base" received over any wordlines. Even if under an extreme stretch of the imagination the IBM openings could be considered as wells, such don't peripherally define "an outline of a memory array area" as required by independent claim 26. Clearly, the IBM storage nodes received within such contact openings include portions which are received laterally outside the opening outlines. Applicant's specification Background section is equally lacking in these regards.

The cited, but unapplied, Dennison et al. Reference is also lacking in these regards.

As each does not disclose that which Applicant recites as argued above, it is inconceivable that the combination could suggest that which Applicant recites in claim 26. Accordingly, the Examiner's rejection of claim 26 over the Background of the Invention and the IBM disclosure is improper and should be withdrawn. Action to that end is requested.

Claims 27-32 depend from claim 26, and are therefore allowable for at least the above reasons regarding claim 26, as well as for their own recited features which are neither shown or supported by the cited art. For example with respect to claims 31 and 32, the Examiner is wrong in concluding that the IBM disclosure teaches that topmost surface of capacitor storage nodes are received elevationally proximate (as Applicant has defined such term) the

insulator layer outermost surface. Indeed, the top surface of the IBM storage nodes are incredibly displaced from the upper surface of the CVD oxide.

Applicant's claim 33 includes at least the same limitations asserted above with respect to claim 26. Accordingly, claim 33 should be allowed for at least the same reasons argued above with respect to claim 26. Action to that end is requested.

Claims 34-37 depend from claim 33, and are therefore allowable for at least the reasons discussed above regarding claim 33, as well as for their own recited features which are neither shown or supported by the cited art.

This application is believed to be in immediate condition for allowance, and action to that end requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, the undersigned respectfully requests a telephone interview prior to issuance of any subsequent action.

Respectfully submitted,

Dated: 2-25-02

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Application Serial No. 09/810,595
Filing Date ..... March 15, 2001
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Group Art Unit 2813
Examiner ..... Yennhu B. Huynh
Attorney's Docket No. MI22-1660
Title: Memory Circuitry (As amended)

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO JANUARY 10, 2002 OFFICE ACTION

In the Specification

The title is amended as follows, underlines indicate insertions and ~~strikeouts~~ indicate deletions.

Memory Circuitry~~, and Dynamic Random Access Memory Circuitry~~

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

34. (Amended) The memory circuitry of claim 33 comprising word lines, wherein the word lines have insulative caps and the well base has a lowest portion which is received at least 2000 Angstroms above the caps.

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